Appl. No. 09/930,804
Amendment Dated: August 1, 2005

Listing of Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently amended): A variable size first in first out (FIFO) memory comprising:

a head FIFO memory including a sequential sprinkler engine for sequentially delivering data packets ~~at a relatively slow rate~~ to a plurality of switching elements at a slow rate relative to the head FIFO memory whereby some latency occurs between said data packets, the switching elements operating at the slow rate;

a tail FIFO memory for storing an overflow of said data packets from said head FIFO memory and for receiving incoming data packets;

both said head FIFO memory and said tail FIFO memory operating at a relatively high data rate equivalent to the rate of the incoming data packets;

a large capacity buffer memory having an effectively lower clock rate than said head FIFO memory and said tail FIFO memory, the large capacity buffer memory for temporarily storing data overflow from said tail FIFO memory;

said head FIFO memory and said tail FIFO memory in combination with said buffer memory forming the variable size FIFO memory.

2. (Previously presented): The variable size FIFO memory as in claim 1 wherein said head and tail FIFO memories each have data blocks of a predetermined and same size and wherein said large

capacity buffer memory has the same size data block as said head and tail FIFO memories to achieve high efficiency data transfer between said head FIFO memory, said tail FIFO memory and said large capacity buffer memory.

3. (Previously presented): The variable size FIFO memory as in claim 1 wherein said head and tail FIFO memories reside on a common semiconductor substrate, and wherein said large capacity buffer memory is remote to the semiconductor substrate.

4. (Previously presented): The variable size FIFO memory as in claim 1 wherein said large capacity buffer memory has a wider bus than a bus included in each of said head and tail FIFO memories.

5. (New): The variable size FIFO memory as in claim 1 wherein said head and tail FIFO memories operate at approximately 10 Gbps and the switching elements operate at approximately 2.5 Gbps.

6. (New): A method for implementing a variable size first in first out (FIFO) memory comprising:

receiving data packets in a tail FIFO memory

providing the data packets to a head FIFO memory

sequentially delivering the data packets from a sprinkler engine included in the head FIFO memory to a plurality of switching elements, the sequentially delivering occurring at a slow rate relative to the head FIFO memory whereby some latency occurs between the data packets;

temporarily storing in the tail FIFO memory a first overflow of the data packets when the head FIFO memory is full;

temporarily storing in a large capacity buffer memory having an effectively lower clock rate than said head FIFO memory and said tail FIFO memory a second overflow of said data packets when the tail FIFO memory is full, wherein both said head FIFO memory and said tail FIFO memory operate at a relatively high data rate equivalent to an incoming rate of the data packets.

7. (New): The method for implementing a variable size FIFO memory as in claim 6 wherein said head and tail FIFO memories each have data blocks of a predetermined and same size and wherein said large capacity buffer memory has the same size data block as said head and tail FIFO.

8. (New): The method for implementing a variable size FIFO memory as in claim 6 wherein said head and tail FIFO memories reside on a common semiconductor substrate, and wherein said large capacity buffer memory is remote to the semiconductor substrate.

9. (New): The method for implementing a variable size FIFO memory as in claim 6 wherein said large capacity buffer memory has a wider bus than a bus included in each of the head FIFO memory and the tail FIFO memory.

10. (New): The method for implementing a variable size FIFO memory as in claim 6 wherein said head and tail FIFO memories operate at approximately 10 Gbps and the switching elements operate at approximately 2.5 Gbps.